to address the language objection, clarify the invention and better define the invention over the art.

Turning now to the art rejections, and considering the rejection of claim 12 under 35 USC § 102(e) as being anticipated by Bothra, U.S. Patent No. 6,010,939, as well as the rejection of claims 13-23 under 35 USC § 103(a) as being unpatentable over Bothra in view of Nitta, et al., U.S. Patent No. 6,225,230, Applicant notes the following:

New claim 33 requires that the shape of at least one of the dummy areas and/or dummy gates be a polygon other than a square or a rectangle. Neither Bothra nor Nitta et al. teaches dummy gates having a shape other than a square or a rectangle. Likewise, new claim 34 requires that the shape of at least one dummy area and/or dummy gate be a circle. Again, neither Bothra nor Nitta et al. teaches dummy areas or dummy gates that are circular in shape. New claim 35 requires that a plurality of dummy areas and/or dummy gates be arranged in at least two rows and/or two columns. Again, neither Bothra nor Nitta et al. teaches dummy areas arranged in rows or columns. New claim 36 requires that at least one of the rows be shifted from another row and/or that at least one column be shifted from another column, once again, a feature taught nowhere in Bothra or Nitta et al.

At pages 4-5 of the Official Action, the Examiner acknowledges that Bothra nowhere teaches the foregoing limitations of claims new 33-36 but attempts to form a 35 USC § 103(a) rejection based on Bothra in combination with the knowledge of one of ordinary skill in the art, citing *In re Daily*, 35 F.2d 699, 149 USPQ 47 (CCPA 1966), for the proposition that the foregoing configurations are merely "a matter of design choice." In *Daily*, no argument was presented to convince the CCPA that a particular configuration of container was significant or anything more than one of numerous configurations. Here, however, the foregoing configurations are a matter of utility, and not design choice. For example, at page 10, lines 3-25,

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701
TEL. 520.882.7623
FAX. 520.882 7643

Applicant explains that improved parasitic capacitance characteristics are provided in a configuration in which the rows and/or columns of dummy areas and/or dummy gates are shifted from one another. This is a feature taught nowhere in the prior art, and is a novel feature of Applicant's invention. Thus, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to come up with the foregoing dummy area/gate configurations.

Moreover, as the Examiner well knows, a combination of references for purpose of a rejection under 35 USC § 103 is proper only if there is some objective teaching in the prior art that would lead one of ordinary skill in the art to combine the relevant teachings of the references. *In re Fine*, 5 USPQ 2d. 1596, 1598 (Fed. Cir. 1988). *See also*, *In re Reinhart*, 189 USPQ 143, 147 (CCPA 1976) ("A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art."). It is submitted that no suggestion or teaching appears in Bothra or Nitta et al. to combine these two references to arrive at Applicant's invention. For prior art references to be combined to render obvious a subsequent invention under 35 USC § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. *Uniroyal v. Rudkin-Wiley*, 5 USPQ 2d. 1434, 1438 (Fed. Cir. 1988). Moreover, even if the teachings of Bothra were combined with Nitta et al., in the manner proposed the Examiner (which itself is still improper absent a suggestion to combine the references), the resulting method or device would not read on Applicant's claims 33-36, as each and every element of Applicant's claims is not taught or disclosed in Bothra and Nitta et al.

For the foregoing reasons, Applicant respectfully submits that the rejections under 35 USC § 102(e) and 35 USC § 103(a) are in error.

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701

TEL. 520.882.7623
FAX. 520.882.7643

Having dealt with all the objections raised by the Examiner, it is believed that the application now is in order for allowance. Early and favorable action are respectfully requested.

In the event the Examiner desires personal contact for further disposition of this case, the Examiner is invited to contact the undersigned attorney at (520) 882-7623.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

RESPECTFULLY SUBMITTED

Norman P. Soloway
Attorney for Applicants
Registration No. 24,315

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231 on May 28, 2002, at Tucson, Arizona.

By Nayat Mostafavi

HAYES SOLOWAY P.C.
130 W. CUSHING ST.
TUCSON, AZ 85701

TEL. 520.882.7623
FAX. 520.882.7643

MARKED COPY OF SPECIFICATION PARAGRAPHS

SERIAL NO. 09/735,005

DOCKET: NEC 444

MARKED SPECIFICATION PARAGRAPHS SHOWING CHANGES MADE

Paragraph beginning at page 2, line 6:

--In the second prior art method, however, when designing a photomask for the dummy gate, [an] additional design time for dummy patterns thereof is required. In particular, if a plurality of kinds of comb-shaped gate patterns are present, the additional design time is enormously large, which would increase the turnaround time, thus increasing the manufacturing cost.--

Paragraph beginning at page 6, line 3:

In the semiconductor device of Figs. 3A, 3B and 3C manufactured by the photomask of Fig. 4, however, when designing the photomask of Fig. 4, an additional design time for the dummy patterns DP is required. In particular, if a plurality of kinds of comb-shaped gate patterns are present, the [additionally] additional designing time [is] would be enormously large, which would increase the turnaround time, thus increasing the manufacturing cost.

Paragraph beginning at page 6, line 11:

A first embodiment of [the] a method for manufacturing a semiconductor device consistent with the invention will be explained next with reference to Figs. 5A, 5B, 5C, 6A, 6B, 6C and 7.

Paragraph beginning at page 6, line 25:

Finally, referring to Fig. 5C, the active area patterns A1 and A2 and the dummy area patterns D are combined [altogether] together to complete the first photomask M1.

Paragraph beginning at page 7, line 3:

Finally, referring to Fig. 6C, the gate patterns GP1 and GP2 and the dummy gate patterns DP are combined [altogether] together to complete the second photomask M2.

Paragraph beginning at page 7, line 17:

The method for manufacturing the semiconductor device of Fig. 7 is explained next with reference to [Figs .] Figs. 8A through 8K, which are cross-sectional views taken along the lines X-X and Y-Y in Fig. 7.

Paragraph beginning at page 7, line 21:

First, referring to Fig. 8A, a monocrystalline silicon substrate 1 is thermally oxidized to form a silicon oxide layer 2 thereon. Then, a silicon nitride layer [2] 3 is deposited on the silicon [nitride] oxide layer [3] 2. Then, a photoresist layer 4 is coated on the silicon nitride layer 3. Then, the photoresist layer 4 is irradiated with ultraviolet light via the photomask M1 of Fig. 5C. Then, the photoresist layer 4 is developed, so that the photoresist layer 4 is patterned.

Paragraph beginning at page 7, line 29:

Next, referring to Fig. 8B, the silicon nitride layer 3 is etched by using the photoresist layer 4 as a mask and the silicon oxide layer 2 as an etching [stopper] stop. Then the silicon oxide layer 2 is etched by using the silicon nitride layer 3 as a mask. Then, the photoresist layer 4 is removed.

Paragraph beginning at page 8, line 6:

Next, referring to Fig. 8E, a CMP process is carried out to flatten the silicon oxide layer 6 using the silicon nitride layer 3 as a [stopper] stop.